IN THE CLAIMS

1. (original) A synchronous Flash memory device comprising:
a memory array;
a control circuit; and
a synchronous memory interface, wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command.

2. (original) The synchronous Flash memory device of claim 1, wherein the external command is received through the synchronous interface.

3. (original) The synchronous Flash memory device of claim 2, wherein the external command is an SDRAM compatible "STOP" command.

4. (original) The synchronous Flash memory device of claim 1, wherein the synchronous interface is an SDRAM or a DDR-SDRAM compatible interface.

5. (original) The synchronous Flash memory device of claim 1, wherein the iterating initialization cycle begins when the power signal on the power bus reaches a predefined trip point.

6. (original) The synchronous Flash memory device of claim 1, wherein the iterating initialization cycle begins a predefined time period after receiving the power signal on the power bus.

7. (original) The synchronous Flash memory device of claim 1, wherein the iterating initialization cycle stops at a random point in the iterating initialization cycle when the external command is received.

8. (original) A memory device comprising:
a memory array;
a control circuit; and
a memory interface, wherein the memory device commences a continuously looping initialization cycle upon receiving a power signal, and stops the continuously looping initialization cycle upon receiving an external signal.

9. (original) The memory device of claim 8, wherein the memory device is a non-volatile memory device.

10. (original) The memory device of claim 8, wherein the memory device is a synchronous Flash memory device.

11. (original) The memory device of claim 8, wherein the memory interface is a synchronous memory interface.

12. (original) The memory device of claim 8, wherein the continuously looping initialization cycle commences when the power signal reaches an identified level.

13. (original) The memory device of claim 8, wherein the continuously looping initialization cycle commences a predefined time period after receiving the power signal.

14. (original) The memory device of claim 8, wherein the continuously looping initialization cycle completes at a random point in the continuously looping initialization cycle when the external signal is received.

15. (original) A synchronous Flash memory device comprising:

a memory array;

a control circuit; and

a synchronous SDRAM compatible memory interface, wherein the synchronous Flash memory device begins a continuously looping initialization cycle upon a power signal on a power bus reaching a specified trip point, and stops the iterating initialization cycle upon receiving an external "STOP" command on the synchronous SDRAM compatible memory interface.

16. (original) A Flash memory device comprising:

a memory array;

a control circuit; and

a memory interface, wherein the Flash memory device begins a continuously looping initialization cycle upon a power signal on a power bus reaching a specified trip point, and stops the iterating initialization cycle upon receiving an external "STOP" command.

17. (original) A method of initializing a synchronous Flash memory device comprising:

commencing a continuously looping initialization cycle upon receiving a power signal; and

stopping the continuously looping initialization cycle upon receiving an external command.

18. (original) The method of claim 17, wherein commencing the continuously looping initialization cycle upon receiving the power signal further comprises commencing the continuously looping initialization cycle upon the received power signal reaching a predetermined value.

19. (original) The method of claim 17, wherein commencing the continuously looping initialization cycle upon receiving the power signal further comprises commencing the

continuously looping initialization cycle upon the received power signal reaching a predetermined value and waiting for a delay period.

20. (original) The method of claim 17, wherein stopping the continuously looping initialization cycle upon receiving the external command further comprises stopping the continuously looping initialization cycle at an in-progress point in the initialization cycle upon receiving the external command.

21. (original) The method of claim 17, wherein receiving the external command further comprises receiving the external command through a synchronous interface.

22. (original) A method of initializing a memory device comprising:
starting a repeating initialization cycle upon receiving a power signal on a power distribution line; and
stopping the repeating initialization cycle upon receiving an external command.

23. (original) The method of claim 22, wherein starting the repeating initialization cycle upon receiving the power signal on the power distribution line further comprises starting the repeating initialization cycle upon the power signal on the power distribution line reaching a predetermined voltage level.

24. (original) The method of claim 22, wherein starting the repeating initialization cycle upon receiving the power signal on the power distribution line further comprises starting the repeating initialization cycle upon the power signal on the power distribution line reaching a predetermined voltage level and waiting a set delay time period.

25. (original) The method of claim 22, wherein stopping the repeating initialization cycle upon receiving the external command further comprises stopping the repeating initialization cycle at a random point in the initialization cycle upon receiving the external command.

26. (original) The method of claim 22, wherein the memory device is a non-volatile memory device.

27. (original) The method of claim 26, wherein the non-volatile memory device is a synchronous Flash memory device.

28. (original) A system comprising:
a host controller; and
a synchronous Flash memory device coupled to the host controller, wherein the synchronous Flash memory device comprises,
a memory array,
a control circuit, and
a synchronous memory interface, wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command.

29. (original) The computer system of claim 28, further comprising a separate external data source.

30. (original) The computer system of claim 29, wherein the separate external data source further comprises a non-volatile memory device.

31. (original) The computer system of claim 29, wherein the separate external data source is coupled to the host controller on a separate bus.

32. (original) The computer system of claim 31, wherein the separate bus is a non-synchronous bus.

33. (original) The computer system of claim 28, wherein the host controller receives software routines to control the synchronous Flash memory device from a non-volatile data source.

34. (Currently Amended) The computer system of claim 33, wherein the non-volatile data source is a non-volatile memory device containing BIOS.

35. (original) The computer system of claim 28, wherein the host controller stops the iterating initialization cycle of the synchronous Flash memory by issuing the external command.

36. (original) The computer system of claim 28, wherein the host controller comprises a processor or an integrated chipset.

37. (original) A computer system comprising:
a host controller; and
a memory device coupled to the host controller, wherein the memory device begins to iterate an initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller.

38. (original) A method of operating a computer system comprising:
coupling a host controller to a memory device;
detecting Vcc in the memory device;
starting an iterating initialization cycle in the memory device; and
stopping iteration of the initialization cycle in the memory device in response to a software command from the host controller.